

IN THE CLAIMS

For the convenience of the Examiner, all pending claims of the present application are shown below whether or not an amendment has been made. Please refer to the attached sheets showing a marked-up version of the amendments to the claims.

1. (Currently Amended) [[C]] A circuit arrangement comprising:

first chips, ~~which each contain~~ containing a transistor and ~~are~~ arranged along a first axis on a first metallic body in a side-by-side and interspaced manner ~~and are~~ electrically connected to ~~the said~~ first body,

second chips~~[[,]]~~ ~~which each contain~~ containing a transistor and ~~are~~ arranged along a second axis parallel to the first axis on a second metallic body in a side-by-side and interspaced manner ~~and are~~ electrically connected to the second body,

wherein the second chips, with regard to a third axis perpendicular to the first axis, ~~each being~~ arranged opposite an area of the first body~~[[,]]~~ ~~which is~~ located between adjacent first chips,

~~wherein~~ the second chips ~~each being~~ electrically connected to ~~the a~~ corresponding opposite area of the first body via at least one bonding connection,

~~wherein~~ the first chips, with regard to the third axis each being arranged opposite an area of the second body, ~~which is~~ located between adjacent second chips,

a third metallic body ~~being~~ arranged on the second body so that it is electrically insulated and having projections, each of which being arranged on one of the areas of the second body, and

~~wherein~~ the first chips each being electrically connected to ~~the an~~ opposite projection of the third body via at least one bonding connection.

2. (Currently Amended) [[C]] A circuit arrangement according to Claim 1, wherein

~~the said~~ first body ~~being~~ connected to an output terminal,

~~the said~~ second body ~~being~~ connected to a voltage terminal, and

~~the said~~ third body ~~being~~ connected to a ground terminal.

3. (Currently Amended) [[C]] A circuit arrangement according to Claim 1, wherein

the first chips without packaging ~~being~~ are directly mounted on the first body in such a way that an electrical contact is created between the first chips and the first body, and

the second chips without packaging ~~being~~ are directly mounted on the second body in such a way that an electrical contact is created between the second chips and the second body.

4. (Currently Amended) [[C]] A circuit arrangement according to Claim 2, wherein the first chips without packaging ~~being~~ are directly mounted on the first body in such a way that an electrical contact is created between the first chips and the first body, and the second chips without packaging ~~being~~ are directly mounted on the second body in such a way that an electrical contact is created between the second chips and the second body.

5. (Currently Amended) [[C]] A circuit arrangement according to Claim 1, further comprising:
a first control line running parallel to the first axis and being connected to the first chips via bonding connections, and
a second control line running parallel to the first axis and being connected to the second chips via bonding connections.

6. (Currently Amended) [[C]] A circuit arrangement according to Claim 2, further comprising:
a first control line running parallel to the first axis and being connected to the first chips via bonding connections, and
a second control line running parallel to the first axis and being connected to the second chips via bonding connections.

7. (Currently Amended) [[C]] A circuit arrangement according to Claim 3, further comprising:
a first control line running parallel to the first axis and being connected to the first chips via bonding connections, and

a second control line running parallel to the first axis and being connected to the second chips via bonding connections.

8. (Currently Amended) ~~[[C]]~~ A circuit arrangement according to Claim 4, further comprising:

a first control line running parallel to the first axis and being connected to the first chips via bonding connections, and

a second control line running parallel to the first axis and being connected to the second chips via bonding connections.

9. (Currently Amended) ~~[[C]]~~ A circuit arrangement comprising:

a first metallic body,

a second metallic body arranged coplanar with said first metallic body,

first chips, ~~which each contain~~ each containing a transistor ~~and are~~ arranged along a first axis on the first metallic body and ~~are~~ electrically connected to the first body,

second chips, ~~which each contain~~ each containing a transistor and ~~are~~ arranged along a second axis parallel to the first axis on the second metallic body and ~~are~~ electrically connected to the second body,

~~wherein~~ the first and second chips ~~are~~ arranged alternative with respect to the first and second axis,

~~wherein~~ the second chips each being electrically connected to ~~the~~ a corresponding opposite area of the first body via at least one bonding connection,

a third metallic body being arranged on the second body so that it is electrically insulated and having projections, each of which being arranged between adjacent second chips on an area ~~one of the areas~~ of the second body, ~~and~~

wherein the first chips each being electrically connected to the opposite projection of the third body via at least one bonding connection.

10. (Currently Amended) ~~[[C]]~~ A circuit arrangement according to Claim 9, wherein ~~the said~~ first body ~~being~~ connected to an output terminal,

~~the said~~ second body ~~being~~ connected to a voltage terminal, and
~~the said~~ third body ~~being~~ connected to a ground terminal.

11. (Currently Amended) [[C]] A circuit arrangement according to Claim 9, wherein
the first chips without packaging ~~being~~ are directly mounted on the first body in such a
way that an electrical contact is created between the first chips and the first body, and
the second chips without packaging ~~being~~ are directly mounted on the second body in
such a way that an electrical contact is created between the second chips and the second body.

12. (Currently Amended) [[C]] A circuit arrangement according to Claim 10,
wherein
the first chips without packaging ~~being~~ are directly mounted on the first body in such a
way that an electrical contact is created between the first chips and the first body, and
the second chips without packaging ~~being~~ are directly mounted on the second body in
such a way that an electrical contact is created between the second chips and the second body.

13. (Currently Amended) [[C]] A circuit arrangement according to Claim 9, further
comprising:
a first control line running parallel to the first axis and being connected to the first chips
via bonding connections, and
a second control line running parallel to the first axis and being connected to the second
chips via bonding connections.

14. (Currently Amended) [[C]] A circuit arrangement according to Claim 10, further
comprising:
a first control line running parallel to the first axis and being connected to the first chips
via bonding connections, and
a second control line running parallel to the first axis and being connected to the second
chips via bonding connections.

15. (Currently Amended) ~~[[C]]~~ A circuit arrangement according to Claim 11, further comprising:

a first control line running parallel to the first axis and being connected to the first chips via bonding connections, and

a second control line running parallel to the first axis and being connected to the second chips via bonding connections.

16. (Currently Amended) ~~[[C]]~~ A circuit arrangement according to Claim 12, further comprising:

a first control line running parallel to the first axis and being connected to the first chips via bonding connections, and

a second control line running parallel to the first axis and being connected to the second chips via bonding connections.